Hindawi Publishing Corporation
Journal of Nanomaterials
Volume 2011, Article ID 906237, 6 pages
doi:10.1155/2011/906237

Research Article

Design and Analysis of a New Carbon Nanotube Full Adder Cell

M. H. Ghadiry,[1] Asrulnizam Abd Manaf,[1] M. T. Ahmadi,[2] Hatef Sadeghi,[2] and M. Nadi Senejani[3]

[1] *School of Electrical and Electronic Engineering, Universiti Sains Malaysia, Engineering Campus, 11800 Penang, Malaysia*
[2] *Faculty of Electrical Engineering, Universiti Teknologi Malaysia, 81310 Skudai, Malaysia*
[3] *Department of Computer Engineering, Islamic Azad University, Ashtian Branch, 39618-13347 Ashtian, Iran*

Correspondence should be addressed to M. H. Ghadiry, m.hoseinghadiry@gmail.com

Received 10 January 2011; Accepted 27 February 2011

Academic Editor: Theodorian Borca-Tasciuc

A novel full adder circuit is presented. The main aim is to reduce power delay product (PDP) in the presented full adder cell. A new method is used in order to design a full-swing full adder cell with low number of transistors. The proposed full adder is implemented in MOSFET-like carbon nanotube technology and the layout is provided based on standard 32 nm technology from MOSIS. The simulation results using HSPICE show that there are substantial improvements in both power and performance of the proposed circuit compared to the latest designs. In addition, the proposed circuit has been implemented in conventional 32 nm process to compare the benefits of using MOSFET-like carbon nanotubes in arithmetic circuits over conventional CMOS technology. The proposed circuit can be applied in very high performance and ultra-low-power applications.

1. Introduction

Fundamental limitations of CMOS technology and anticipations of Moore's law have motivated researchers to find suitable alternative for these devices. Among several proposed alternatives [1–5], carbon nanotube field effect transistors seem to be a promising successor for CMOS devices due to their superior characteristics [1, 6]. CNFETs indicate great potential further than silicon nanoelectronic, and significantly illustrate greater performance than conventional CMOS models specially in case of switching energy. Large transconductance of CNFETs creates huge interest in nanoelectronic circuits' application as well. As a result, many works have been done to model their properties [5–12]. Several HSPICE models for CNFETs have been presented so far such as [6, 8]. Among several SPICE models for CNFET, only in [6] practical device, nonidealises, and more than one tubes are modelled.

CNFETs' high performance and low power consumption properties make them interesting to be used in the design of low-power-demanding arithmetic circuits. One of the most important blocks of these circuits is full adder cell [13–20], which are duplicated many times in building up larger circuits. In this paper, CNFET technology has been employed, to make a very high-performance and ultra-low-power adder from the proposed design. Only three CNTFET-based full adder cells have been presented so far [19, 21–23]. However, parasitic capacitances and layout effects have not been considered in them. In addition, all of those designs are based on adjusting threshold voltage (V_t) by manipulating diameter of tubes, which demands complex and expensive fabrication process [24, 25]. As a result, in addition to attempting to achieve the least PDP among the most state-of-the-art designs in the literature, these two issues have been addressed in this work by using the same diameter and threshold voltage for all devices and drawing postlayout for every design based on a tailored industrial fabrication process [26, 27]. Moreover, the design is immune against misaligned tubes fabrication defect [27].

2. Transistor Level Design Methodology

In practice, full adders are idle most of the time. In addition, in deep submicron technologies, static power is not as negligible as it was in technologies higher than 0.18 μm. One way to reduce static power consumption and delay is full-swing design. However, it usually requires a high number

Table 1: Truth table of the cout module as a multiplexer.

Switch control	In1	In2	Out
$h = 0$	$a = 1$		cout = 1
$h = 1$		$c = 1$	cout = 1
$h = 1$		$c = 0$	cout = 0
$h = 0$	$a = 0$		cout = 0

of transistors, which in turn increases power consumption. Therefore to achieve full-swing outputs with minimum transistor count, the highest performance, and the lowest static power consumption, a new method has been applied to all three, sum, cout, and XOR-XNOR modules. In order to show how the method works, design of cout module is verified here, which is the same approach that has been applied to sum and xor-xnor modules as well.

As (1) shows, both cout and sum can be expressed based on h and $\overline{h}$. Therefore, we used h and $\overline{h}$ as common intermediate signals to implement sum and cout modules using the proposed method:

$$\begin{aligned} \text{sum} &= a \oplus b \oplus c, \\ \text{sum} &= \left(\overline{a \oplus b}\right)\left(\overline{a \oplus b}\right) \cdot c + (a \oplus b) \cdot \overline{c}, \\ \text{sum} &= \overline{h} \cdot c + h \cdot \overline{c}, \\ \text{cout} &= ab + a\,c + bc, \\ \text{cout} &= \left(\overline{a \oplus b}\right) \cdot a + (a \oplus b) \cdot c, \\ \text{cout} &= \overline{h} \cdot a + h \cdot c. \end{aligned} \tag{1}$$

This method relies on design of multiplexers using pass transistors. Table 1 shows the truth table of the cout module as a multiplexer with h as its switch control, a and c as its inputs, and cout as its output.

As Table 1 shows, each input has two states, and thus four outputs are possible, two of which are logic 1 and two logic 0. Two rules must be followed in order to have full-swing outputs.

(1) To design for logic 1 outputs, P-doped tubes must be used in series and all triggering signals, switch control and inputs, must be logic 0.

(2) To design for logic 0 outputs, N-doped tubes must be used in series and all triggering signals must be logic 1.

Therefore, in the first two rows of Table 1 there must be no logic 1 as input and in the last two rows no logic 0. As a result, Table 2 is obtained by inverting inconsistent signals.

The result is shown in Table 3, which determines the selected signals and consequent logic to design cout module.

Consequently, four submodules must be designed, two of which are shown in Figure 1.

Each of them has two versions. Those with connections to VDD and GND can be implemented directly based on Table 3, and they are able to boost the input signals. Those with no connection to VDD or GND can be designed using complement of inputs 1 and 2 as VDD and GND connections. The later designs use less area compared to the former version. However, they levy high delay if they are used in carry propagation path. Thereby, in the proposed circuits (AFS, CNTAFS), cout module has been designed using connections to VDD and GND, while xor-xnor and sum have been designed using the second approach in order to reduce the power consumption.

Table 2: Result of applying mentioned rules on Table 1.

Switch control	In1	In2	Out
$h = 0$	$\overline{a} = 0$		cout = vdd
$\overline{h} = 0$		$\overline{c} = 0$	cout = vdd
$h = 1$		$\overline{c} = 1$	cout = gnd
$\overline{h} = 1$	$\overline{a} = 1$		cout = gnd

Table 3: Required logic, transistor type, and inputs to implement full-swing cout module.

Submodule	Switch control	In1,2	Logic	Transistor type
1	h	$\overline{a}$	$h \cdot \overline{a}$	PMOS
2	$\overline{h}$	$\overline{c}$	$\overline{h} \cdot \overline{c}$	PMOS
3	h	$\overline{c}$	$h \cdot \overline{c}$	NMOS
4	$\overline{h}$	$\overline{a}$	$\overline{h} \cdot \overline{a}$	NMOS

3. Proposed Design

Figure 2 shows the proposed design using the demonstrated method. In this design, h and $\overline{h}$ can be generated simultaneously by applying proper transistor sizing in order to reduce glitches and unnecessary power consumption in subsequent submodules. Using no feedback transistor is one reason of low power consumption and low delay of this module compared to similar designs with feedback transistor such as Hybrid [28]. In addition, using no VDD and GND in xor-xnor and sum modules contributes to power consumption reduction. Applying $\overline{a}$ as input adds two transistors to the circuit. However, reusing this signal in cout module helps decrease its adverse effect on power consumption and area. Furthermore, there are only two transistors between each supply rail and cout node, which results in low delay in cascaded mode. Module sum uses only 4 transistors, which reduces power consumption.

4. Layout Design

Based on the proposed method in [27], current industrial processes can be used to design compact and simple layouts for CNFET-based circuit with minor modifications. Following design rules has been considered in layout drawing (see Table 4). Other technology rules such as Polysilicon and metal routing can remain valid for simplicity and reusability. In addition, using this method provides layouts, which are immune to miss-positioned tubes [27]. Furthermore, in this method, there is no need for neither using undoped or etched regions nor using via on top of active region.

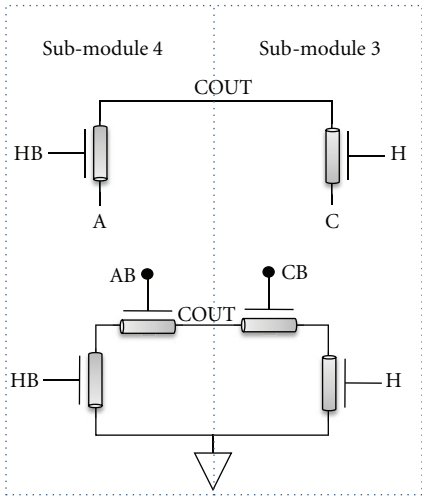

Figure 1: Submodules 3 and 4 of the module cout using the proposed method.

Table 4: Sample design rules used to design layout for CNFET-based circuit.

Design rule	Description	Value
Ls/Ld	Length of source/drain	3λ
Lgs/Lgd	Distance between gate and source/drain	2λ
Lg	Length of gate	2λ

As shown in Figure 3 tailored 32 nm MOSIS process has been employed on layout design of the CNFET-based circuit. Standard 32 nm process has been used to design layouts of CMOS-based circuits. Parasitic capacitances for both CNFET-based and CMOS-based circuits have been extracted and included in simulations.

5. Simulation Environment

In order to show advantages of the proposed circuit over existed adders in the literature, the proposed circuits have been compared with several circuits from the literature. CMOS [14] as basic circuit for comparison in standard CMOS technology and Hybrid [28] as one of the best circuits in terms of power and performance are also implemented in standard CMOS. There are only five CNTFET-based adders in the literature, all of which have been compared with our design. Design 1 [21], design 1 in [22], which is the same as design 2 in [21], the proposed adder in [22], and the presented full adder in [19] are called CNTD1, CNTD2, CNTD3, and CNTD4 in this paper.

Eight cells of each mentioned full adder have been cascaded to make an 8-bit ripple carry adder. All inputs come from input buffers, which are two cascaded inverters in the same technology. The W/L (width/length) ratios for inverters are made to be equal to 5/3 and 12/5. In CNFET devices, these values are 4 and 8 tubes per device, respectively. Other parameters of CNFET devices are the same as the default values for semiconducting tube [6]. Transistor sizing has been done to achieve the best PDP in each circuit. In case of CNFET device, the number of tubes has been changed in order to gain the best PDP. To generate input patterns and consider the worst cases in all designs, the same method as [29] has been used in this work to identify the critical path of each design to spot the longest delay.

The performance and PDP of the under test circuits have been evaluated based on worst-case propagation delay. Propagation delay is calculated from 50% of input voltage level to 50% of output voltage level. Rise time and fall time of input signals in all simulations are 5% of the input signal's pulse width. As adder circuits are idle most of the time we calculated $P_{20\%}$ based on formula $P_{20\%} = 0.2P_{\text{active}} \times 0.8P_{\text{Idle}}$, where the active power is the power consumption of the circuit when inputs are triggered at 300 MHz frequency and idle power is the average static power of the circuit for several combinations of inputs. Area has been calculated by multiplication of total height and width of the circuits' postlayout. CNFET model presented in [6] has been applied in this research, and simulations have been carried out using HSPICE.

6. Results and Discussion

Table 5 shows the result of simulation for 8-bit ripple carry adder (RCA) including parasitic capacitances and nonidealises of both Carbon nanotube and CMOS devices. Symbol Φ in Table 5 shows that product of PDP and area. Apparently, the proposed circuit in CNFET technology (CNAFS) outperforms the other circuits in terms of PDP. This is due to full-swing design of the xor-xnor module with low number of transistors, which reduces leakage current in both itself and subsequent modules and improves the delay compared to other circuits. In addition, boosting power of cout module contributes to more delay reduction. Module sum has low driving ability but low power consumption. As it plays no role in critical path, low power consumption is more important than high driving capability on its design.

Comparing the proposed CNFET-based with CMOS-based (AFS) circuits reveals that PDP has been improved at least 8 times. In terms of area, although drawing layout using the method proposed in [27] has some limitations, the area is still less than that of AFS. CNAFS with 1 GHz maximum operating frequency and 1.17 μw power consumption is the fastest circuit and lowest power-consuming circuit among all simulated circuits. Other CN-based designs, CNTD1–4, have higher PDP than our design mostly because of large input capacitances imposing high delay. In order to gain the least PDP transistor sizes must be scaled up, which cause higher power consumption. CNTD1 shows high static power due to use of ratio logic in its design. Using 4 inverters in CNTD4 contributes to high power consumption. However, its delay is slightly less than CNAFS due to boosting power of these inverters.

Table 6 shows power and performance of the proposed circuit at 0.6 and 0.9 V supply voltage. By decreasing VDD from 0.9 V to 0.6 V, PDP of CNAFS increased from 1.17 to 1.57, while it increased from 9.88 to 17.58 for AFS. In other words, CNFET-based design is less sensitive to voltage variation than CMOS-based one.

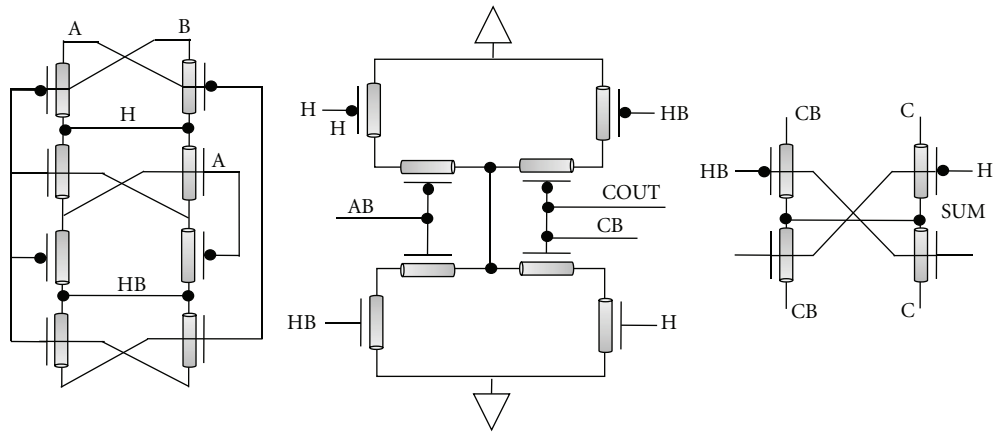

Figure 2: The proposed full adder cell implemented with CNFET.

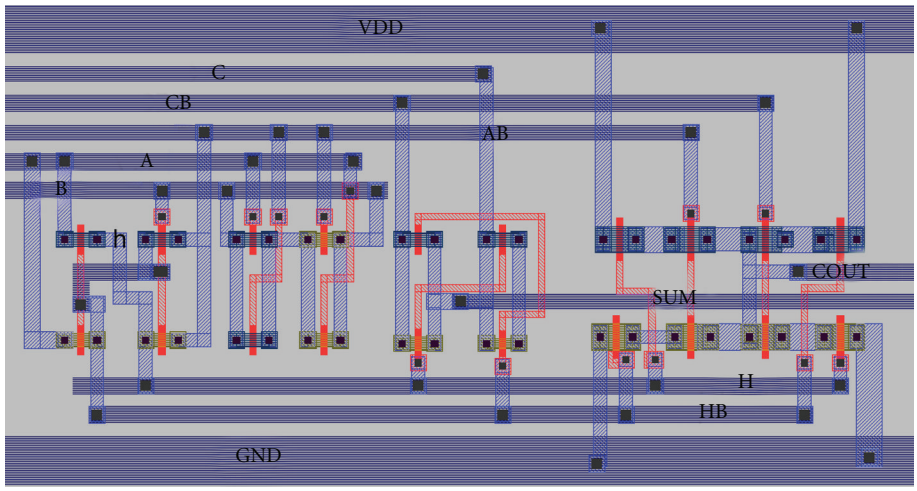

Figure 3: Misaligned CNT immune layout of the proposed design.

However, analysis of those circuits for different loads shows that CNFET-based circuit lacks driving large loads. As Figure 4 shows, for loads larger than almost 90 fF, CMOS-based circuit has lower PDP than CNFET-based circuit. It is worth mentioning that output load is mostly smaller than 90 fF in practical applications in 32 nm process.

7. Conclusions

A new full adder cell has been proposed based on a new method to design full-swing low-power high-performance circuits. The proposed method has been used to design a new full adder cell. The results showed that the proposed full adder has lower power and higher performance than other basic and newly presented full adders. In addition, the proposed design has been implemented using CNFETs, and the postlayout of the design has been provided using modified standard 32 nm technology from MOSIS. The results indicated that the proposed CNFET-based circuit is much faster and also its power consumption is much less than those of the COMS-based counterparts. Comparing the proposed full adder to CMOS full adder revealed that

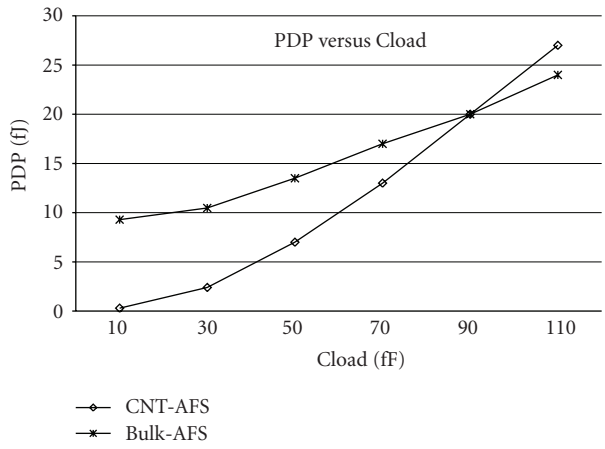

Figure 4: The effect of output load on PDP of the proposed circuit in both CNFET and CMOS technologies.

the presented circuit's PDP is far more less than that of CMOS. Evaluating the proposed circuit at different supply

Table 5: Simulation results for 8-bit ripple carry adder at 0.9 V supply voltage, 20 fF output load, and 300 MHz input frequency.

Circuit	P_{VDD} (μw)	P_{input} (μw)	P_{active} (μw)	P_{idle} (μw)	$P_{20\%}$ (μw)	Delay (ns)	PDP (fJ)	Area (μm^2)	Φ (pJ×μm^2)	No Dev.	1/delay (GHz)
CNT-AFS	5.67	0.2	5.87	0.002	1.18	0.995	1.17	6.1	0.0071	24	1005
CNTD4	7.4	0.33	7.73	0.012	1.56	0.91	1.42	5.7	0.0081	18	1099
CNTD3	6.9	0.21	7.11	0.008	1.43	0.9	1.29	4.4	0.0057	13	1111
CNTD2	8.5	0.44	8.94	0.015	1.80	1.1	1.98	5.5	0.0109	15	909
CNTD1	15.3	0.7	16.00	0.15	3.32	1.04	3.45	16.4	0.0566	13	962
AFS	17.3	7.235	24.54	0.88	5.61	1.76	9.88	10.0	0.10	24	568
CMOS	28.9	13.545	42.45	1.64	9.80	1.26	12.35	13.0	0.16	28	794
Hybrid	29.395	10.6	40.00	1.17	8.94	1.92	17.16	9.9	0.17	24	521

Table 6: Simulation results for different VDDs with 300 MHz input frequency and 20 fF output load.

Circuit	VDD = 0.6			VDD = 0.9		
	$P_{20\%}$ (μw)	Delay (ns)	PDP (fJ)	$P_{20\%}$ (μw)	Delay (ns)	PDP (fJ)
CNT-AFS	0.63	2.79	1.75	1.18	0.995	1.17
CNTD4	0.83	2.55	2.12	1.56	0.91	1.42
CNTD3	0.77	2.45	1.8	1.43	0.9	1.29
CNTD2	0.96	3.08	2.96	1.80	1.1	1.98
CNTD1	1.78	2.91	5.17	3.32	1.04	3.45
Bulk-AFS	3.00	4.93	14.79	5.61	1.76	9.88

voltages revealed that CNFET-based circuit's PDP is less dependent on VDD than the same circuit in conventional CMOS technology. However, analysing the proposed full adder in both CMOS and CNFET technologies in high fan-out situation showed that the CNFET-based circuit's PDP has been impaired more than that of the same circuit in CMOS technology, which shows lack of CNTs in driving large loads. Nevertheless, results indicated that CNAFS outperforms at loads smaller than 90 fF, which is acceptable in 32 nm process.

Acknowledgments

This work has been supported by PhD fellowship scheme with no. 1/11 and grant numbered 304/PELECT/60310023 from school of electrical and electronic engineering, Universiti Sains Malaysia.

References

[1] Y. M. Lin, J. Appenzeller, J. Knoch, and P. Avouris, "High-performance carbon nanotube field-effect transistor with tunable polarities," *IEEE Transactions on Nanotechnology*, vol. 4, no. 5, pp. 481–489, 2005.

[2] A. Raychowdhury, A. Keshavarzi, J. Kurtin, V. De, and K. Roy, "Carbon nanotube field-effect transistors for high-performance digital circuits—DC analysis and modeling toward optimum transistor structure," *IEEE Transactions on Electron Devices*, vol. 53, no. 11, pp. 2711–2717, 2006.

[3] A. M. Ionescu, "Electronic devices: nanowire transistors made easy," *Nature Nanotechnology*, vol. 5, no. 3, pp. 178–179, 2010.

[4] J. P. Colinge, C. W. Lee, A. Afzalian et al., "Nanowire transistors without junctions," *Nature Nanotechnology*, vol. 5, no. 3, pp. 225–229, 2010.

[5] M. Taghi Ahmadi, H. Houg Lau, R. Ismail, and V. K. Arora, "Current-voltage characteristics of a silicon nanowire transistor," *Microelectronics Journal*, vol. 40, no. 3, pp. 547–549, 2009.

[6] J. Deng and H.-S. P. Wong, "A compact SPICE model for carbon-nanotube field-effect transistors including nonidealities and its application—part II: full device model and circuit performance benchmarking," *IEEE Transactions on Electron Devices*, vol. 54, no. 12, pp. 3195–3205, 2007.

[7] M. T. Ahmadi, R. Ismail, M. L. P. Tan, and V. K. Arora, "The ultimate ballistic drift velocity in carbon nanotubes," *Journal of Nanomaterials*, vol. 2008, no. 1, Article ID 769250, 2008.

[8] C. Dwyer, M. Cheung, and D. J. Sorin, "Semi-empirical SPICE models for carbon nanotube FET logic," in *Proceedings of the 4th IEEE Conference on Nanotechnology*, pp. 386–388, August 2004.

[9] M. Hayatia, A. Rezaeia, and M. Seifia, "CNT-MOSFET modeling based on artificial neural network: application to simulation of nanoscale circuits," *Solid-State Electronics*, vol. 54, pp. 52–57, 2010.

[10] M. Ahmadi, J. F. Webb, Z. Johari, and R. Ismail, "Single wall carbon nanotube field effect transistor model," *Journal of Computational and Theoretical Nanoscience*, vol. 8, no. 2, pp. 261–267, 2011.

[11] M. T. Ahmadi, Z. Johari, N. A. Amin, A. H. Fallahpour, and R. Ismail, "Graphene nanoribbon conductance model in parabolic band structure," *Journal of Nanomaterials*, vol. 2010, Article ID 753738, 4 pages, 2010.

[12] M. T. Ahmadi, M. L. P. Tan, R. Ismail, and V. K. Arora, "The high-field drift velocity in degenerately-doped silicon nanowires," *International Journal of Nanotechnology*, vol. 6, no. 7-8, pp. 601–617, 2009.
[13] M. H. Ghadiry, H. Mohammadi, and M. N. Senejani, "Two new low power high performance full adder with minimum gates," *International Journal of Electrical and Information Engineering*, vol. 3, pp. 124–131, 2009.
[14] K. Navi, M. Maeen, V. Foroutan, S. Timarchi, and O. Kavehei, "A novel low-power full-adder cell for low voltage," *Integration, the VLSI Journal*, vol. 42, no. 4, pp. 457–467, 2009.
[15] V. Foroutan, K. Navi, and M. Haghparast, "A new low power dynamic full adder cell based on majority function," *World Applied Sciences Journal*, vol. 4, pp. 133–141, 2008.
[16] M. Nadi, M. H. Ghadiry, and M. K. Dermany, "The effect of number of virtual channel on NOC EDP," *Journal of Applied Mathematics & Informatics*, vol. 2010, pp. 539–551, 2010.
[17] M. H. Ghadiry, A. Khari, and M. N. Senejani, "A new full-swing full adder based on new logic approach," *World Applied Sciences Journal*, vol. 1, 2011.
[18] M. H. Ghadiry, A. K. A'Ain, and M. N. Senejani, "Design and analysis of a novel low PDP full adder cell," *Journal of Circuits, Systems, and Computers*, vol. 20, 2011.
[19] K. Navi, M. Rashtian, A. Khatir, P. Keshavarzian, and O. Hashemipour, "High speed capacitor-inverter based carbon nanotube full adder," *Nanoscale Research Letters*, vol. 5, no. 5, pp. 859–862, 2010.
[20] M. N. Senejani, M. Hosseinghadiry, and M. Miryahyaei, "Low dynamic power high performance adder," in *Proceedings of International Conference on Future Computer and Communication (ICFCC '09)*, pp. 482–486, April 2009.
[21] K. Navi, A. Momeni, F. Sharifi, and P. Keshavarzian, "Two novel ultra high speed carbon nanotube Full-Adder cells," *IEICE Electronics Express*, vol. 6, no. 19, pp. 1395–1401, 2009.
[22] K. Navi, R. S. Rad, M. H. Moaiyeri, and A. Momeni, "A low-loltage and energy-efficient full adder cell based on carbon nanotube technology," *Nano-Micro Letters*, vol. 2, pp. 114–120, 2010.
[23] K. Navi, M. Maeen, V. Foroutan, S. Timarchi, and O. Kavehei, "A novel low-power full-adder cell for low voltage," *Integration, the VLSI Journal*, vol. 42, no. 4, pp. 457–467, 2009.
[24] C. V. Nguyen, Q. Ye, and M. Meyyappan, "Carbon nanotube tips for scanning probe microscopy: fabrication and high aspect ratio nanometrology," *Measurement Science and Technology*, vol. 16, no. 11, pp. 2138–2146, 2005.
[25] C. Wang, J. Zhang, K. Ryu, A. Badmaev, L. G. de Arco, and C. Zhou, "Wafer-scale fabrication of separated carbon nanotube thin-film transistors for display applications," *Nano Letters*, vol. 9, no. 12, pp. 4285–4291, 2009.
[26] 2011, http://www.mosis.com/ibm/ibm_processes.html.
[27] S. Bobba, J. Zhang, A. Pullini, D. Atienza, and G. De Micheli, "Design of compact imperfection-immune CNFET layouts for standard-cell-based logic synthesis," in *Proceedings of Design, Automation and Test in Europe Conference and Exhibition (DATE '09)*, pp. 616–621, April 2009.
[28] S. Goel, A. Kumar, and M. A. Bayoumi, "Design of robust, energy-efficient full adders for deep-submicrometer design using hybrid-CMOS logic style," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 14, no. 12, pp. 1309–1321, 2006.
[29] J. F. Lin, Y. T. Hwang, M. H. Sheu, and C. C. Ho, "A novel high-speed and energy efficient 10-transistor full adder design," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 54, no. 5, pp. 1050–1059, 2007.